FORM PTO-1390 (REV 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. P107242-00019
	TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	DATE: July 9, 2001
		U.S. APPLN. NO. (IF KNOWN, SEE 37 C.F.R. 1.5) 09/868901
INTERNATIONAL APPLICATION NO. PCT/JP00/07641	INTERNATIONAL FILING DATE October 31, 2000	PRIORITY DATE CLAIMED November 11, 1999

TITLE OF INVENTION: SILICON SINGLE CRYSTAL WAFER AND MANUFACTURING PROCESS THEREFOR

APPLICANT(S) FOR DO/EO/US: Masaro TAMATSUKA

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371. (THE BASIC FILING FEE IS ATTACHED)

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures [35 U.S.C. 371(f)] at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper demand for International Preliminary Amendment was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed [35 U.S.C. 371(c)(2)]
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☒ A translation of the International Application into English [35 U.S.C. 371(c)(2)].

7. ☐ Amendments to the claims of the International Application under PCT Article 19 [35 U.S.C. 371(c)(3)]
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 [35 U.S.C. 371(c)(3)].

9. ☒ An oath or declaration of the inventor(s) [35 U.S.C. 371(c)(4)].

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 [35 U.S.C. 371(c)(5)].

Items 11 - 16 below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    CHECK NO. 321203
    Drawings (5 sheets)
    International Search Report
    Japanese Language Request Form
    Notification of Receipt of Record Copy (PCT/IB/301)
    Notification Concerning Submission of Priority Documents (PCT/IB/304)
    Notice Informing the Applicant of the Communication of the International Application to the Designated Offices (PCT/IB/308)
    International Publication No. WO 01/34882 A1

U.S. APPL'N. NO. (IF KNOWN SEE 37 C.F.R. 1.5) 09/868901	INTERNATIONAL APPLICATION NO. PCT/JP00/07641	ATTORNEY DOCKET NO. P107242-00019 DATE: July 9, 2001

17. ☐ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
Basic National Fee [37 C.F.R. 1.492(a)(1)-(5)]:		
Search Report has been prepared by the EPO or JPO.....$860.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482).....$690.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO [37 C.F.R. 1.445(a)(2)].....$710.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) or international search fee [37 C.F.R. 1.445(a)(2)] paid to USPTO.....$1,000.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(e)].	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	8 - 20 =	0	X $ 18.00	$	
Independent Claims	2 - 3 =	0	X $ 80.00	$	
Multiple dependent claim(s) (if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 860.00	
Reduction by one-half for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28). -				$	
SUBTOTAL =				$ 860.00	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(f)]. +				$	
TOTAL NATIONAL FEE =				$ 860.00	
Fee for recording the enclosed assignment [37 C.F.R. 1.21(h)]. The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 900.00	
				Amount to be refunded	$
				Charged	$

a. ☒ A check in the amount of $900.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 01-2300 in the amount of $ to cover the above fee.
A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2300.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive [37 C.F.R. 1.137(a) or (b)] must be filed and granted to restore the application to pending status.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TAMATSUKA

Serial No.: New Application

Group Art Unit:

Filed: July 9, 2001

Examiner:

For: SILICON SINGLE CRYSTAL WAFER AND MANUFACTURING PROCESS THEREFOR

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

July 9, 2001

Sir:

Prior to calculation of the filing fee and prior to the examination of this application, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-6 and add the following claims.

-- 7. (Added) A silicon single crystal wafer which is a wafer prepared by means of a Czochralski method, the silicon single crystal comprising at least one portion formed of an OSF ring portion in contact with a boat on which the silicon single crystal is placed for heat treatment.

8. (Added) A silicon single crystal wafer according to claim 7, wherein the OSF ring region is an annular region with a width of 10 mm or less from a periphery of the silicon single crystal wafer.

9. (Added) A silicon single crystal wafer according to claim 7, wherein a nitrogen concentration in the silicon single crystal wafer is in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$.

10. (Added) A silicon single crystal wafer according to claim 8, wherein a nitrogen concentration in the silicon single crystal wafer is in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$.

11. (Added) A manufacturing process for a silicon single crystal wafer comprising the steps of:

growing a silicon single crystal rod by means of a Czochralski method in a condition that an OSF ring region is formed in a peripheral region of the silicon single crystal rod; and

slicing the grown silicon signal crystal rod into silicon single crystal wafers.

12. (Added) A manufacturing process for a silicon single crystal wafer according to claim 11, wherein a condition under which the OSF ring region is formed in a peripheral region of the silicon single crystal rod is such that when a pulling rate is indicated by F [mm/min] and an average temperature gradient in a pulling direction in a length

between points corresponding to a silicon melting point and 1400°C in the crystal is indicated by G [°C/mm] by definition, there is present in a peripheral region of the crystal, an OSF ring region of a defect distribution chart which shows defect distribution, with an abscissa representing a distance [mm] in a direction to the crystal periphery from the center and an ordinate representing a value of F/G [mm^2/°C min].

13. (Added) A manufacturing process for a silicon single crystal wafer according to claim 11, wherein when a silicon single crystal rod is grown by means of the Czochralski method, the silicon single crystal rod is pulled while doping the silicon single crystal rod with nitrogen at a concentration in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$.

14. (Added) A manufacturing process for a silicon single crystal wafer according to claim 12, wherein when a silicon single crystal rod is grown by means of the Czochralski method, the silicon single crystal rod is pulled while doping the silicon single crystal rod with nitrogen at a concentration in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$. --

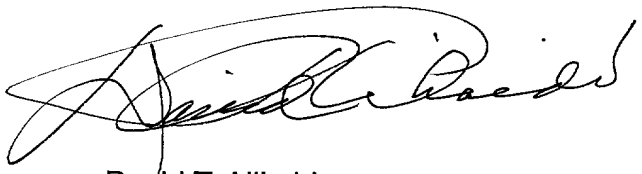
REMARKS

The above amendments to the claims have been made to correct the multiple dependency of the claims and to put the application in better condition for examination. No new matter has been added.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2300.

Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC



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DESCRIPTION

SILICON SINGLE CRYSTAL WAFER AND MANUFACTURING PROCESS THEREFOR

Technical Field

This invention relates to a silicon single crystal wafer and a manufacturing process therefor, and particularly, to a silicon single crystal wafer capable of suppressing growth of slip dislocations easily generated in a heat treatment step and a manufacturing process therefor.

Background Art

An integrated circuit such as LSI has been fabricated mainly starting with a silicon single crystal wafer prepared by means of a pulling method called Czochralski method (CZ method) through many production steps. As one of the production steps, there exists a heat treatment step. There is very important the heat treatment step where, for example, oxide film formation on a wafer surface, impurity diffusion, formation of a defect free layer and a gettering layer and others are performed.

There are known two types of furnaces, vertical and horizontal, as a so-called batch type resistance heating heat treatment furnace which is used in the heat treatment step, and capable of heat treating many wafers at one time. The horizontal furnace is to heat treat wafers which are vertically placed on a jig called a boat for holding them and inserted into the interior thereof. The vertical furnace is to heat treat wafers which are horizontally

placed on a boat and inserted into the interior thereof.

One of problems in the heat treatment step is generation of slip dislocations. A slip dislocation means a defect having a stepwise profile created on a wafer surface by slip deformation in crystal due to a thermal stress during the heat treatment step. When such slip dislocations generate on a wafer surface, not only a mechanical strength is reduced, but device characteristics such as junction leakage are adversely affected; therefore, it is desired to reduce slip dislocations to the lowest possible level.

When heat treatment is conducted using the batch type heat treatment furnace as described above, temperature distribution is generated in a wafer during loading it into and unloading it from the furnace or during raising or lowering a furnace temperature, which causes a stress in the wafer due to the temperature distribution. Further, when this stress exceeds a critical value, a slip dislocation generates. In this case, since a wafer is placed on a boat, the wafer weight is apt to be concentrated at a contact portion with the boat, which causes a bigger stress acting on the contact portion and easier generation of slip dislocations. Especially, when a wafer is of a larger diameter, the wafer weight becomes bigger and influences greatly.

On the other hand, there is also a case where, in the heat treatment step, an RTA (Rapid Thermal Annealing) apparatus is employed, which is a single wafer heat treatment furnace using lamp heating or the like, in addition to the above described batch type heat treatment furnace. In the case of an apparatus of this kind, since the furnace is a single wafer processing type and a temperature up and down rate is very fast and temperature distribution in a wafer is harder to occur compared with the

batch type heat treatment furnace, the furnace is useful in heat treatment of a large diameter wafer, but there is a phenomenon that slip dislocations are easy to occur at a contact portion with a jig on which wafers are placed because a stress due to the wafer weight is concentrated to the contact portion, which is similar to the case of the batch type heat treatment furnace.

In order to suppress slip dislocations generated in such a way, remedies have been mainly studied from two viewpoints in the prior art. An approach from one viewpoint is to reduce a stress imposed on a contact portion between a wafer and a boat, wherein the concentration of a stress is alleviated by improving a shape of the boat. For example, a technique disclosed in JP-A-97-251961 is such that an angle of the wafer placing portion of the boat for a vertical furnace heat treatment is held is set so as to be in conformity with deformation thereof caused by the wafer weight, and thereby a contact portion between the wafer and the boat is altered from a condition of a point contact to a plane contact, with the result that concentration of a stress is prevented.

Another approach is to reduce temperature distribution in a wafer generated in a heat treatment step by improving a heating condition. For example, a technique disclosed in JP-A-95-235507 is such that hydrogen or helium having higher thermal conductivity than nitrogen or argon which is usually used during raising and lowering temperature in a heat treatment step is employed to encourage thermal conduction to a wafer so as to reduce a temperature difference in a wafer surface. Also, a proposal has been made in JP-A-95-312351 that generation of slip dislocations is prevented by reducing a temperature rise/fall rate with a rise in temperature.

As approaches from the two viewpoints, not limited to the above described examples, many others are known. While all the above described approaches have some level of effectiveness for suppressing slip dislocations in a heat treatment step, they are not necessarily perfect as remedies for all of a variety of heat treatment steps and furthermore, some of them are not practical in cost problems.

On the other hand, in addition to approaches from the above described two viewpoints to suppress generation of slip dislocations, one attempt has been tried very recently in which characteristics of a wafer itself are improved to make slip resistance better. For example, in JP-A-97-227290 there is proposed a wafer in which an oxygen concentration in the peripheral region is not less than 95 % of that in the middle on the basis of observation that a silicon single crystal wafer prepared from a single crystal rod grown by means of a CZ method has a lower oxygen concentration in the peripheral region than in the middle, which is a cause for generation of slip dislocations. A manufacturing process for such a wafer is disclosed in the publication in which a single crystal rod of a diameter larger than that of a product wafer by 10 mm or more is pulled and the single crystal is ground off to a target diameter.

Further, description is found in JP-A-97-190954 that in a CZ wafer of a low oxygen concentration generation of slip dislocations is suppressed when polyhedral oxide precipitates are formed at a prescribed density in a region with a width of 10 mm or less from the periphery where slip dislocations are generated with ease.

Furthermore, in order to generate the oxide precipitates at the

prescribed density, the publication discloses a technique in which oxygen is ion-implanted in the region with a width of 10 mm or less from the periphery, and two stage heat treatment is carried out in a nitrogen atmosphere.

However, since the techniques described above are to improve characteristics of a wafer itself, an effect may be obtained in all the heat treatment steps, but any of them lacks practical use due to insufficient simplicity and cost performance. That is, in the technique disclosed in JP-A-97-227290, a loss of a silicon single crystal rod increases and further an extra time required for processing becomes necessary, and in JP-A-97-190954, additional steps of ion implantation and two stage heat treatment are required.

The invention has been made in light of the above described problems and it is accordingly an object of the invention to provide a CZ silicon single crystal wafer to be subjected to a heat treatment step which has improved slip resistance of a portion in contact with a heat treatment boat by using a manufacturing process with extreme simplicity, convenience, and very low cost.

Disclosure of the Invention:

In order to achieve the object, a silicon single crystal wafer of the invention is a wafer prepared by means of a Czochralski method, and characterized in that when the silicon single crystal wafer is placed on a boat for heat treatment, at least a portion of the silicon single crystal wafer in contact with the boat is formed of an OSF ring region. When a silicon single crystal wafer has a portion formed of the OSF ring region in contact with the

boat, growth of a slip dislocation is confined within the interior (the bulk portion) of the wafer, if the slip dislocation generates at the contact portion; therefore, no slip dislocation extends to the wafer surface and no influence is exerted on a device region in the surface side of the wafer.

Furthermore, the OSF ring region is preferably an annular region with a width of 10 mm or less from a periphery of a silicon single crystal wafer. This is because if the OSF ring region expands inward up to a distance more than 10 mm from the periphery, a useful area in which characteristically excellent devices can be fabricated is reduced, leading to a case where a sufficient number of product devices cannot be ensured. In case of a vertical furnace, since the contact portion between the wafer and the boat is located at about 8 mm at most from the periphery of the wafer, the OSF ring located at about 10 mm from the periphery is effective for suppressing growth of the slip dislocation. On the other hand, in case of a horizontal furnace, since the contact portion between the wafer and the boat is at about 3 mm at most from the periphery, the OSF ring located even at about 5 mm from the periphery is still effective for suppressing growth of the slip dislocation.

Moreover, a nitrogen concentration in a silicon single crystal wafer is preferably in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$. A wafer including nitrogen in such a content is more effective for suppressing growth of slip dislocations since sizes of oxide precipitates decrease and a density thereof increases due to effects of nitrogen.

Also, a nitrogen concentration is desirably 1×10^{10} / cm^3 or more in order to increase a density of oxide precipitates, and preferably 5×10^{15} / cm^3

or less in order not to hinder crystallization of a silicon single crystal, but more preferably in the range of 1 x 10^{12} to 1 x $10^{15}/cm^3$ in terms of suppression of slip dislocations.

In order to produce such a silicon single crystal wafer, a manufacturing process for a silicon single crystal wafer of the invention is characterized in that a silicon single crystal rod is grown by means of a Czochralski method in a condition that an OSF ring region is formed in a peripheral region of the silicon single crystal rod and the silicon signal crystal rod obtained is sliced into silicon single crystal wafers.

A detailed pulling condition can be such that when a pulling rate is indicated by F [mm/min] and an average temperature gradient in a pulling direction in a length between points corresponding to a silicon melting point and 1400°C in the crystal is indicated by G [°C/mm] by definition, there is present in a peripheral region of the crystal, an OSF ring region of a defect distribution chart showing defect distribution with an abscissa representing a distance [mm] in a direction to the crystal periphery from the center and an ordinate representing a value of F/G [mm^2/°C·min].

Moreover, when a silicon single crystal rod is grown by means of the Czochralski method, if the silicon single crystal rod is pulled while doping with nitrogen at a concentration in the range of 1 x 10^{10} to 5 x 10^{15} / cm^3, a silicon single crystal wafer doped with nitrogen at a concentration in the range of 1 x 10^{10} to 5 x 10^{15} / cm^3 can be produced.

Brief Description of the Drawings:

Fig. 1 is sectional views schematically showing the state of generation of slip dislocations in a contact portion between a wafer of the

invention and a boat;

Fig. 2 is schematic drawings showing results of X ray topography in Examples and Comparative Examples of the invention;

Fig. 3 is a chart schematically showing the state of generation of an OSF ring region at different pulling rate of crystals;

Fig. 4 is a defect distribution chart with an abscissa representing a distance in a direction to the crystal periphery from the center and an ordinate representing a value of F/G when a silicon single crystal of the invention is pulled; and

Fig. 5 is a schematic and descriptive view of a single crystal pulling apparatus of a CZ method used in the invention.

Best mode for Carrying out the Invention:

Description will be given of embodiments of the invention below. The inventor of the invention has investigated into slip dislocations in a silicon single crystal wafer prepared from a silicon single crystal rod pulled under various pulling conditions, generated mainly from a contact portion between a boat and the silicon single crystal wafer when the silicon single crystal wafer is subjected to heat treatment. The investigation has uncovered the fact that a wafer whose contact portion with a boat is included in an OSF ring region has low generation of slip dislocations and a slip dislocation thus generated, if any, does not extend to a wafer surface which is the surface of the side opposite to the contact portion. Based on this finding, the present inventor has completed the present invention.

Here, description will be given of an OSF ring region.

A CZ wafer prepared from a silicon single crystal rod pulled by means of a CZ method is subjected to oxidation and then, defects called OSF (Oxidation-Induced Stacking Fault) are sometimes generated in the form of a ring. This region is called an OSF ring region. It is assumed that fine oxide precipitates (about 30 nm) which are introduced in this region during crystal growth work as nuclei and interstitial silicon atoms aggregate on the nuclei to form OSF to be observed during subsequent oxidation treatment.

Fig. 3 is a chart schematically showing the state of generation of an OSF ring region at different pulling rates of crystals. According to Fig. 3, it is found that as a pulling rate is reduced, a ring diameter decreases and with further reduction in the pulling rate, the ring disappears at the center of the crystal (Shinoyama, et al., Applied Physics, Vol. 60, No. 8 (1991) pp. 766 to 773).

Therefore, the state of generation of an OSF ring region is dependent on a crystal growth condition, from which it is understood that if a crystal growth condition is controlled, an OSF ring region can be formed in a desired position.

Note that it is confirmed according to a most recent research that in the upper and lower parts sandwiching the OSF region therebetween in Fig. 3 (inner and outer parts of the OSF region), there are regions called N-regions in which no or very few crystal defects caused by vacancies and interstitial silicon atoms are present (JP-A-99-147786). Besides, the further inside of the N-region inside of the OSF region (a higher pulling rate side in the chart) is called a V-rich region, rich in defect caused by vacancies, and the further outside of the N-region outside of the OSF region (a lower pulling rate

side in the chart) is called an I-rich region, rich in defect caused by interstitial silicon atoms (Fig. 4).

Fig. 1 is to simply express a concept of the invention, where schematically shown is the state of generation of slip dislocations at a contact portion between a wafer and a boat.

Fig. 1(a) shows a case of a wafer having no OSF region, wherein slip dislocations generated at the contact portion extend to a wafer surface. On the other hand, Fig. 1(b) shows a case where a contact portion resides in an OSF ring region, wherein even when slip dislocations occur, none of the slip dislocations extend to a wafer surface. While Fig. 1 shows a case of a vertical furnace, in case of a horizontal furnace as well, growth of slip dislocations is effectively suppressed when a contact portion between a wafer and a boat resides within an OSF region.

It is not clear the reason why slip dislocations are hard to be generated in an OSF regions or growth of slip dislocations is confined within the interior of a wafer and thereby the dislocations are hard to reach a wafer surface side, but since it is said that fine oxide precipitates serving as OSF nuclei reside in the OSF region as described above and interstitial silicon atoms are excessively included throughout all of the region (Takao Abe, Silicon-Crystal Growth and Wafer Processing-, Baifu Kan, p. 296), it is considered that oxide precipitates and silicon interstitial atoms take part in the above phenomenon.

Further, it is also known that when nitrogen is doped into a silicon single crystal, effects arise that aggregation of atomic vacancies in silicon is suppressed to reduce sizes of crystal defects and that oxygen precipitation is

accelerated. Therefore, it is considered that when the OSF region is formed in a peripheral region of a wafer with nitrogen doping, a density of fine oxide precipitates serving as OSF nuclei can be increased in the peripheral region, thereby enhancing an effect of suppressing slip dislocations.

Next, description will be given of an exemplary structure of a single crystal pulling apparatus of a CZ method used in the invention with reference to Fig. 5. As shown in Fig. 5, the silicon single crystal pulling apparatus 30 includes: a pull chamber 31; a crucible 32 placed in the pull chamber 31; a heater 34 surrounding the crucible 32; a crucible support shaft 33 rotating the crucible 32 and a rotation mechanism therefor (not shown); a seed chuck 6 holding a silicon seed crystal 5; a wire 7 pulling up the seed chuck 6; and a take-up mechanism (not shown) rotating or winding up the wire 7. The crucible 32 is provided with a quartz crucible in the inner side which contains a silicon melt 2 and a graphite crucible in the outer side. Furthermore, the heater 34 is surrounded with a heat insulating member 35.

Besides, in order to set manufacturing conditions relating to a manufacturing process of the invention, a solid/liquid interface heat insulating member 8 of an annular shape surrounds the solid/liquid interface of the crystal and a top surrounding heat insulating member 9 is further provided thereon. The solid/liquid interface heat insulating member 8 is disposed above a silicon melt 2 with a gap 10 of 3 to 5 cm between the low end thereof and a melt surface 3. The top surrounding heat insulating member 9 is not used on certain pulling conditions. Moreover, there may be provided a cylindrical cooling apparatus (not shown) for cooling the single crystal by blowing cooling gas or shielding the radiant heat.

In recent years, there has also been employed in many cases a so-called MCZ method where magnets (not shown) have been disposed outside the pull chamber 31 in the horizontal direction and by applying a magnetic field with a horizontal direction, a vertical direction or other directions to the silicon melt 2, convection of the melt is suppressed to ensure stable growth.

Next, description will be given of a method for growing a single crystal using the single crystal pulling apparatus 30.

A high purity polycrystalline silicon starting material is melted in the crucible 32 by heating the material at the melting point thereof (about 1420℃) or higher. At this time, in a case where nitrogen is doped, for example a silicon wafer or wafers each formed with a nitride film thereon is put into the crucible 32 in advance. Then, by reeling out the wire 7, a tip end of the seed crystal 5 is put into contact with or dipped into the silicon melt 2 almost at the center of the surface of the melt 2. Subsequent to this, not only the crucible support shaft 33 is rotated in a proper direction, but the wire 7 is also wound up while rotating, with the result that the seed crystal is pulled up, whereby growth of a single crystal gets started. Thereafter, the single crystal rod 1 of an almost cylindrical shape can be obtained by properly adjusting a pulling rate and temperature.

In the invention, pulling conditions are so adjusted that a region called OSF ring region described above is formed in a peripheral region of the silicon single crystal rod 1. For example, in case of using a specific furnace structure such as a generating position of an OSF ring region can be controlled by altering a pulling rate of the single crystal as shown in Fig. 5,

the pulling rate may be controlled so as to generate the OSF region in a peripheral region of the single crystal. The OSF region preferably covers in an annular region with a width of 10 mm or less from the periphery of the wafer.

However, in order to stably generate an OSF ring region only in the peripheral region of a crystal simply by only controlling a pulling rate, strict control of the pulling rate comes to be required. Therefore, when a furnace structure is adjusted by using a heat insulating member or a cooling apparatus to control a temperature gradient in the vicinity of a solid/liquid interface of a pulling crystal, a generation distribution of an OSF region in Fig. 3 can be altered. In such a case, when as in the case of Fig. 4, a pulling rate is indicated by F [mm/min], there is indicated by G [°C/mm] an average temperature gradient of the crystal in a pulling direction in a length between points corresponding to a silicon melting point and 1400°C, and a value of F/G [mm^2/°C·min] is used as a parameter, conditions under which an OSF ring region is formed in the peripheral region of a crystal can be controlled with a sufficient control margin.

When a single crystal rod is pulled such that an OSF ring region resides in the peripheral region of the single crystal rod as stated above and thus obtained rod is processed by means of an ordinary wafer process, there are obtained wafers each having an OSF ring region in a wafer peripheral region in which a contact between the wafer and a boat is easy to occur in a heating process.

That is, since there can be obtained wafers capable of suppressing generation of slip dislocations only by controlling a generating position of an

OSF ring region during crystal pulling, the manufacturing process is very effective for reducing a cost without a need for an increase in processing loss and the number of additional steps.

Concrete description will be given of embodiments of the invention below taking up examples, but it should be understood that the invention is not limited to the examples.

(Example 1)

With the pulling apparatus 30 shown in Fig. 5, a starting material polycrystalline silicon was charged in a 20 inch quartz crucible to pull a p-type silicon single crystal rod with a < 100 > orientation and a diameter of 6 inches. In this case, a F/G value in the central portion of the crystal was controlled in the range of 0.25 to 0.33 $mm^2/°C \cdot min$ to form an OSF ring region in an annular region with a width of about 10 mm or less from the periphery of the crystal. Furthermore, control was performed such that a nitrogen concentration in the pulling crystal fell in the range of 5×10^{13} to $1 \times 10^{14}/cm^3$, based on the calculation, by adding wafers each formed with a silicon nitride film into the starting substance polycrystalline silicon.

Wafers were cut from the single crystal obtained here and an ordinary wafer process was applied to prepare mirror polished wafers. The mirror polished wafers were inserted into a vertical furnace to perform heat treatment on the wafers in an argon atmosphere at 1150°C for one hour, followed by further heat treatment to simulate device fabrication on the wafers: firstly, at 800°C for 4 hours in a nitrogen atmosphere and secondly, at 1000°C for 16 hours in a dry oxygen atmosphere. Subsequent to this, presence or absence of slip dislocations and positions of an OSF ring region

were confirmed by means of X-ray topography. The heat treatment at 1150°C for one hour in an argon atmosphere was performed in conditions of a load/unload temperature of 850°C, a boat speed of 15 cm/min, a temperature rise rate of 10°C/min and a temperature fall rate of 5°C/min and the heat treatment to simulate device fabrication was performed such that after the heat treatment of 1000°C, the temperature was reduced down to 800°C and thereafter, the wafers were taken out from the furnace. A quartz boat was used in the heat treatment. A position in which an OSF ring region occurred were confirmed by judging a pattern of oxygen precipitation since the oxygen precipitation is harder to occur in the OSF ring region than the other regions. Results thereof were shown as a schematic drawing in Fig. 2(a). No slip dislocation was observed as shown in Fig. 2(a). Note that the OSF ring region was formed in an annular region with a width a little less than 10 mm from the periphery of a wafer.

(Example 2)

With the pulling apparatus 30 shown in Fig. 5, a starting material polycrystalline silicon was charged in a 20 inch quartz crucible to pull a p-type silicon single crystal rod with a < 100 > orientation and a diameter of 6 inches without doping nitrogen. In this case, a F/G value in the central portion of the crystal is controlled in the range of 0.18 to 0.22 $mm^2/°C \cdot min$ to form an OFS ring region in an annular region with a width of about 10 mm or less from the periphery of the crystal.

Wafers were cut from the single crystal obtained here and an ordinary wafer process was applied to prepare mirror polished wafers. The same heat treatment as in Example 1 was applied to the thus obtained

mirror polished wafers to perform observation by means of X-ray topography. Results thereof are described in Fig. 2(b).

As a result, it was found that slip dislocations of a length of about 7 mm occurred from a contact portion with a boat. A wafer after the observation by means of X-ray topography was etched by a fluoric acid and nitric acid based preferential etching liquid and thereafter, the wafer was observed on a surface to confirm presence or absence of pits corresponding to slip dislocations by means of an optical microscope with the result that no pit of slip dislocations was observed and it was confirmed that no slip dislocation extended up to a surface of the wafer. Note that an OSF ring region was formed in an annular region with a width a little less than 10 mm from the periphery of the wafer.

(Comparative Example 1)

With the pulling apparatus 30 shown in Fig. 5, a starting material polycrystalline silicon was charged in a 20 inch quartz crucible to pull a p-type silicon single crystal rod with a < 100 > orientation and a diameter of 6 inches without doping nitrogen. In this case, the single crystal was pulled at a growth rate F of about 1.6 mm/min in a condition where no OFS ring region was formed.

Wafers were cut from the single crystal obtained here and an ordinary wafer process was applied to prepare mirror polished wafers. The same heat treatment as in Example 1 was applied to the thus obtained wafers to perform observation by means of X-ray topography. Results thereof are described in Fig. 2(c).

As a result, it was found that slip dislocations of a length of about 15

mm occurred from a contact portion with a boat. A wafer was etched by a preferential etching liquid as in Example 2 and thereafter, the wafer was observed on a surface by means of an optical microscope with the result that pits of slip dislocations were observed and it was confirmed that slip dislocations extended up to a surface of the wafer.

It is found from the results of Fig. 2 that if a wafer has a contact portion formed of an OSF ring region between the wafer and a boat, perfectly no slip dislocation occurs or at least growth of slip dislocations can be suppressed even when the wafer is subjected to high temperature heat treatment in which slip dislocations are easily generated.

(Examples 3 and 4, and Comparative Example 3)

Mirror polished wafers obtained from the same silicon single crystals used in Examples 1 and 2, and Comparative Example 1, respectively, were used to perform heat treatment in a horizontal furnace. Heat treatment was performed similar to that of Example 1: heat treatment on the wafers in an argon atmosphere at 1150°C for one hour, followed by further heat treatment to simulate device fabrication on the wafers: firstly, at 800°C for 4 hours in a nitrogen atmosphere and secondly, at 1000°C for 16 hours in a dry oxygen atmosphere. The heat treatment at 1150°C for one hour in an argon atmosphere was performed in conditions of a load/unload temperature of 950°C, a boat speed of 15 cm/min, a temperature rise rate of 6°C/min and a temperature fall rate of 3°C/min and the heat treatment to simulate device fabrication was performed such that after the heat treatment of 1000°C, the temperature was reduced down to 800°C and thereafter, the wafers were taken out from the furnace. A quartz boat was used in the heat treatment.

Presence or absence of slip dislocations in wafers having been subjected to the heat treatment and positions of OSF ring regions thereon were confirmed by X-ray topography.

No slip dislocation was observed on wafers prepared from the same silicon single crystal as used in Example 1.

Slip dislocations of a length of about 4 mm were generated from a contact portion with a boat on a wafer (Example 4) prepared from the same single crystal as used in Example 2. However, preferential etching was performed on a wafer as in Example 2 and a wafer surface thus etched was observed by means of an optical microscope, with the result that while some pits were present in the vicinity of a contact portion with a boat, no pit corresponding to slip dislocations was observed in the inner surface of a annular region with a width of 2 mm from the periphery and further, the effect of suppressing growth of slip dislocations by an OSF ring region was confirmed. Note that on wafers of Examples 3 and 4, OSF ring regions were formed in annular regions each with a width a little less than 10 mm from the periphery of the wafers.

In wafers (Comparative Example 2) prepared from the same single crystal as used in Comparative Example 1, slip dislocations of a length of about 20 mm from a contact portion with a boat were generated. Preferential etching was performed similar to Example 2 to observe a wafer surface with an optical microscope and as a result, pits corresponding to slip dislocations were observed in a portion in which slip dislocations had been observed by means of X ray topography.

Capability of Exploitation in Industry

According to the invention, there can be suppressed slip dislocations which easily occur in a contact portion between a boat and a silicon single crystal wafer which is subjected to a variety of heat treatment steps with a simple and convenient method and in addition, since no need arises to increase processing loss and the number of steps, a silicon single crystal wafer with high slip resistance can be provided at a low cost and thereby, a value in terms of industrial applicability is great.

CLAIMS

1. A silicon single crystal wafer which is a wafer prepared by means of a Czochralski method characterized in that when the silicon single crystal wafer is placed on a boat for heat treatment, at least a portion of the silicon single crystal wafer in contact with the boat is formed of an OSF ring region.

2. A silicon single crystal wafer according to claim 1, wherein the OSF ring region is an annular region with a width of 10 mm or less from a periphery of the silicon single crystal wafer.

3. A silicon single crystal wafer according to claim 1 or 2, wherein a nitrogen concentration in the silicon single crystal wafer is in the range of 1×10^{10} to $5 \times 10^{15}/cm^3$.

4. A manufacturing process for a silicon single crystal wafer characterized in that a silicon single crystal rod is grown by means of a Czochralski method in a condition that an OSF ring region is formed in a peripheral region of the silicon single crystal rod and the grown silicon signal crystal rod is sliced into silicon single crystal wafers.

5. A manufacturing process for a silicon single crystal wafer according to claim 4, wherein a condition under which the OSF ring region is formed in a peripheral region of the silicon single crystal rod is such that when a pulling rate is indicated by F [mm/min] and an average temperature gradient in a pulling direction in a length between points corresponding to a silicon melting point and 1400°C in the crystal is indicated by G [°C/mm] by definition, there is present in a peripheral region of the crystal, an OSF ring region of a defect distribution chart which shows defect distribution, with an

abscissa representing a distance [mm] in a direction to the crystal periphery from the center and an ordinate representing a value of F/G [$mm^2/°C \cdot min$].

6. A manufacturing process for a silicon single crystal wafer according to claim 4 or 5, wherein when a silicon single crystal rod is grown by means of the Czochralski method, the silicon single crystal rod is pulled while doping the silicon single crystal rod with nitrogen at a concentration in the range of 1×10^{10} to 5×10^{15} / cm^3.

ABSTRACT

There is provided a manufacturing process for a CZ silicon single crystal wafer which is subjected to heat treatment wherein slip resistance of a portion of the CZ silicon single crystal wafer in contact with a heat treatment boat is improved with extreme simplicity, convenience and very low cost. A silicon single crystal rod is grown by means of a Czochralski method in a condition that an OSF ring region is formed in a peripheral region of the silicon single crystal rod and the grown silicon signal crystal rod is processed into silicon single crystal wafers, whereby the silicon single crystal wafer is obtained such that when the silicon single crystal wafer is subjected to heat treatment, at least a portion of the silicon single crystal wafer in contact between the wafer and the boat is formed of an OSF ring region.

FIG. 1

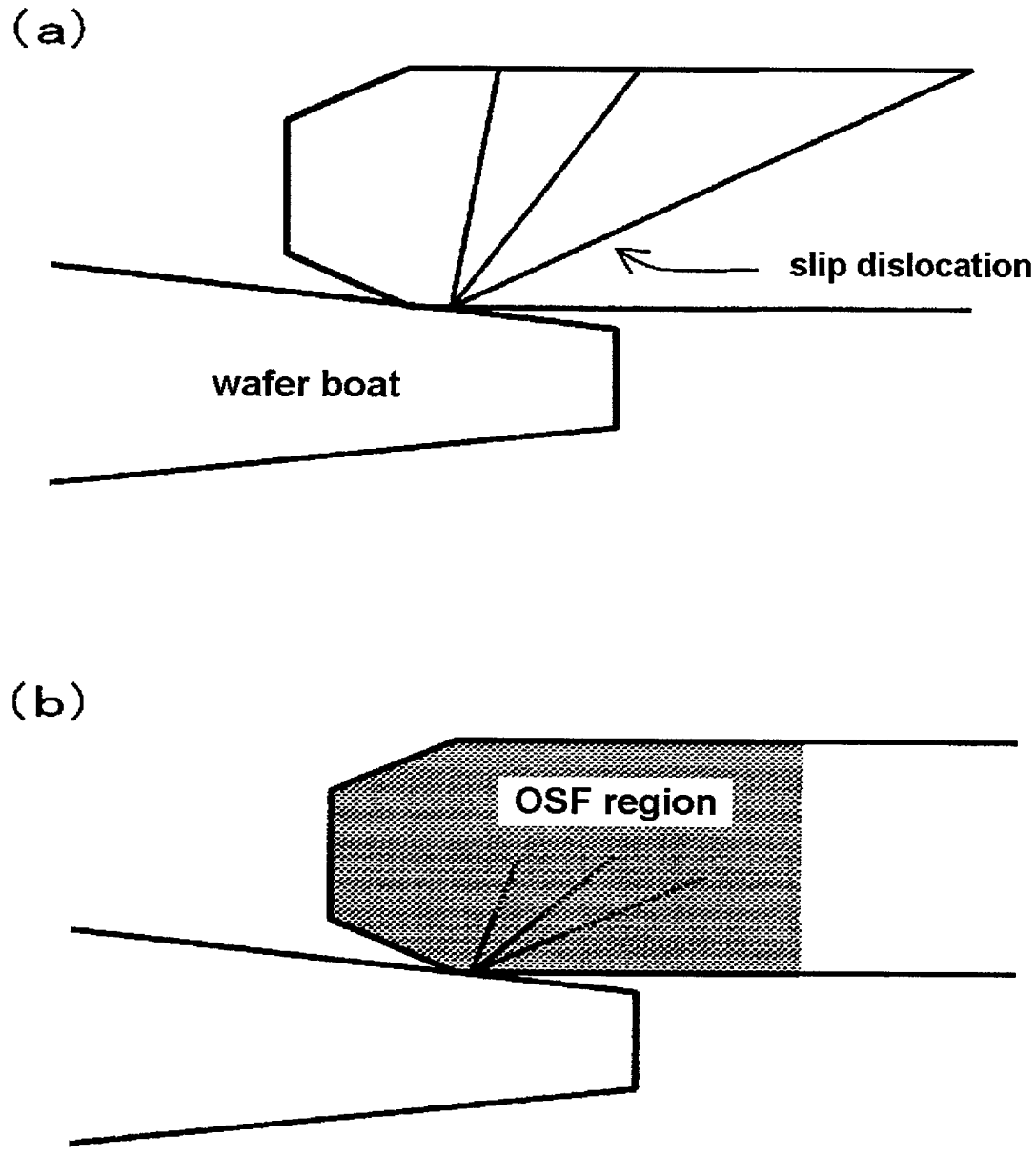
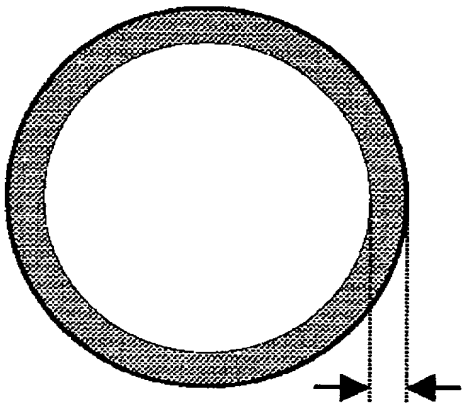
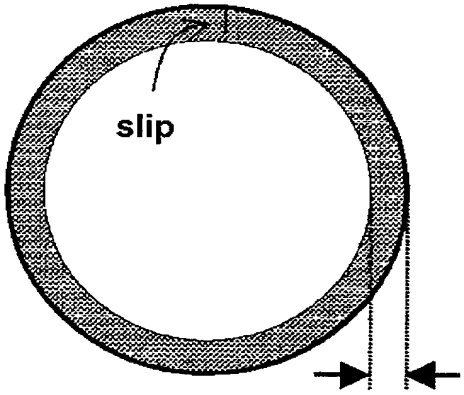


FIG. 2

(a) nitrogen doped, with OSF



(b) nitrogen undoped, with OSF



(c) nitrogen doped, without OSF

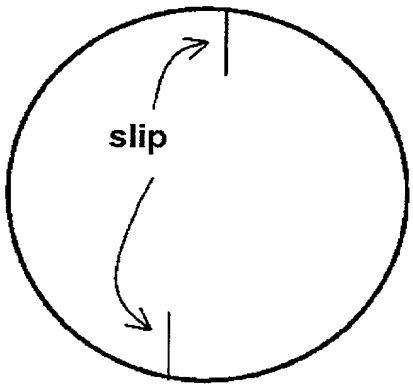


FIG.3

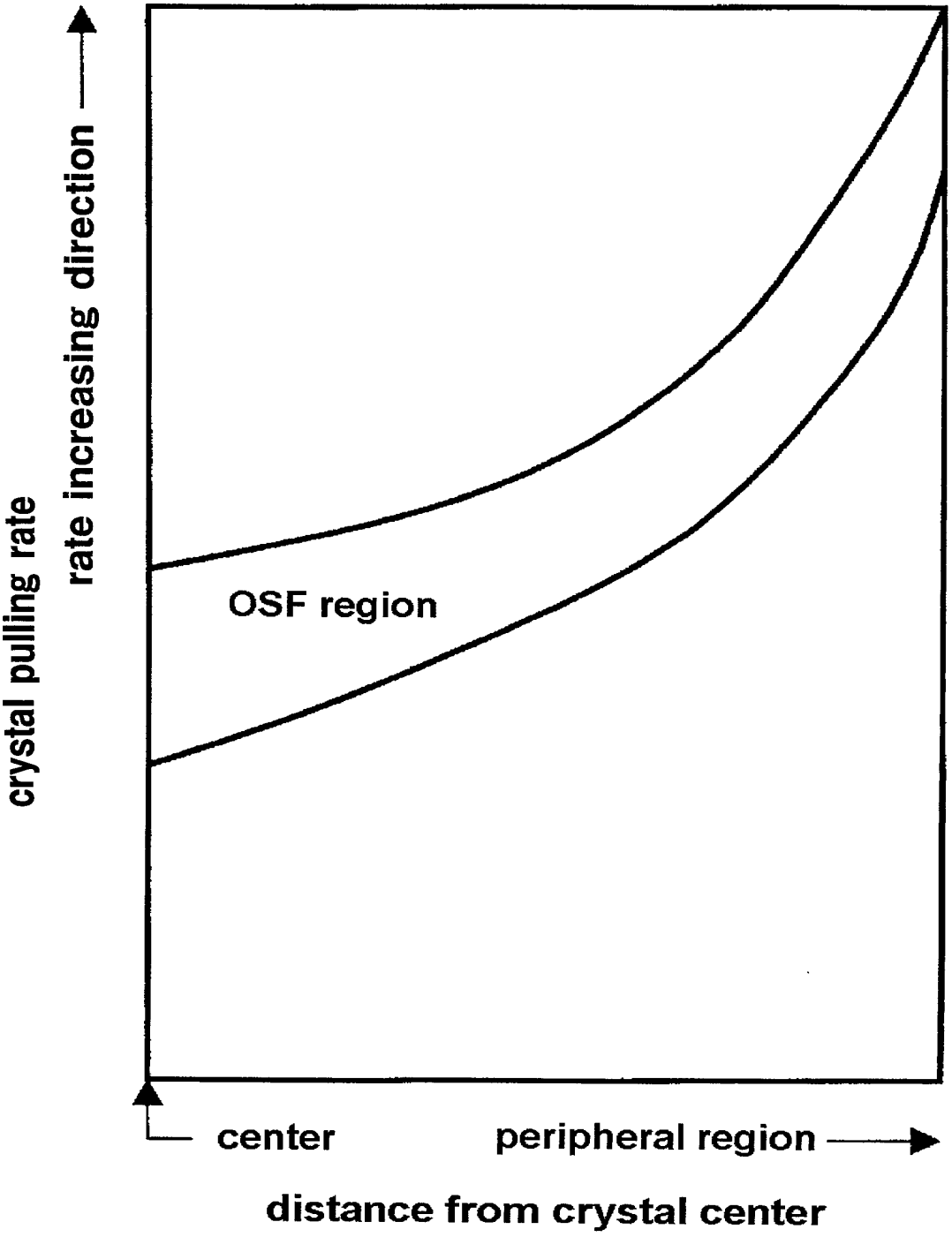


FIG. 4

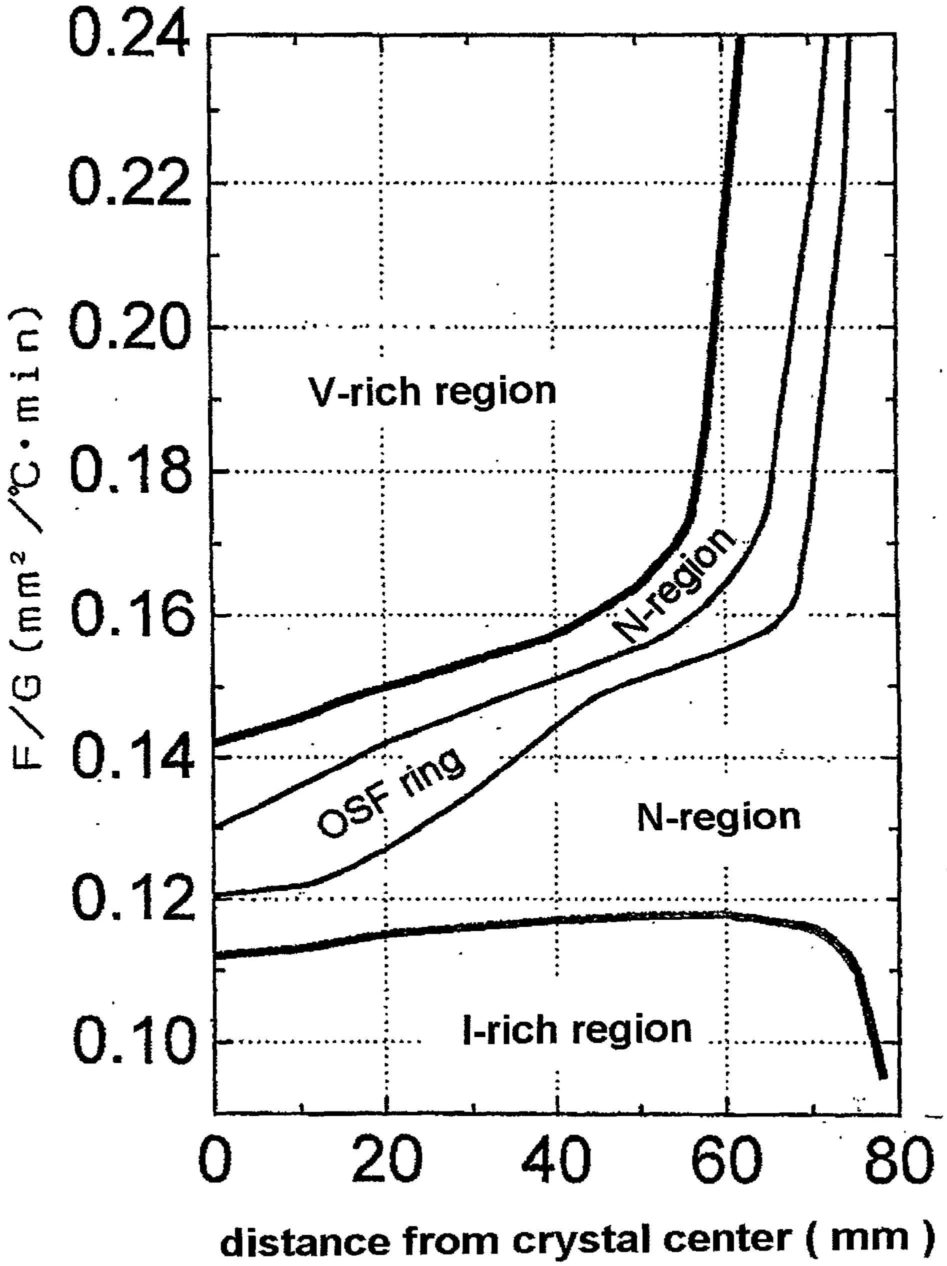
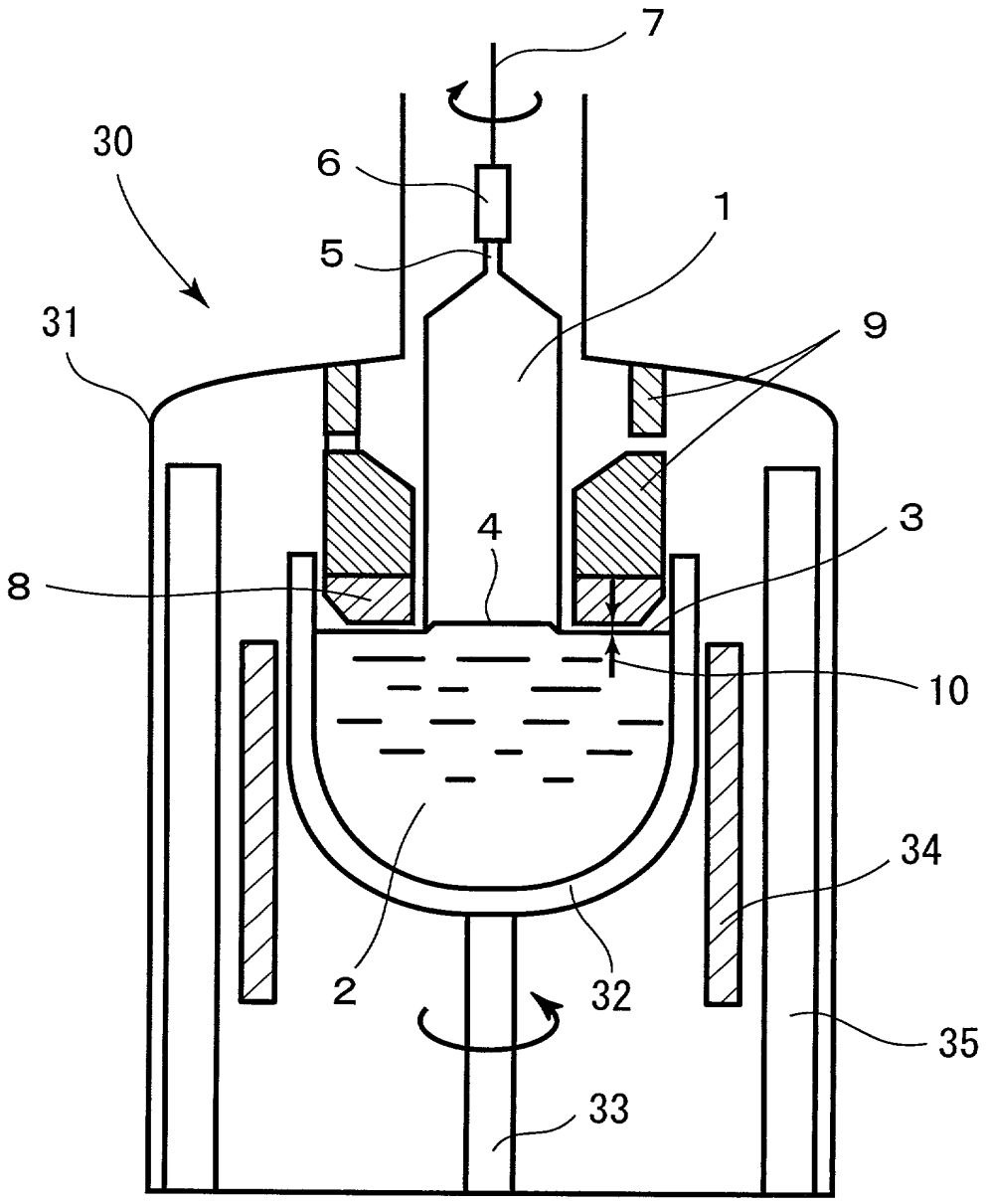

0.24
0.22
0.20
0.18
0.16
0.14
0.12
0.10
F/G (mm² /℃・min)
V-rich region
N-region
OSF ring
N-region
I-rich region
0
20
40
60
80
distance from crystal center (mm)

FIG. 5



PTO/SB/106 (8-96)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SILICON SINGLE CRYSTAL WAFER AND MANUFACTURING PROCESS THEREFOR

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on October 31, 2000 as United States Application Number or PCT International Application Number PCT/JP00/07641 and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11-320507	JAPAN	11/11/1999	☐
			☐

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(Application No.) (出願番号)	(Filing Date) (出願日)

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

書類送付先

15

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. ~~25,895~~; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Monica Chin Kitts, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; James A. Poulos, III, Reg. No. 31,714; Patrick D. Muir, Reg. No. 37,403; Sharon N. Klesner, Reg. No. 36,335; Murat Ozgu, Reg. No. 44,275; Bradley D. Goldizen, Reg. No. 43,637, and N. Alexander Nolte, Reg. No. 45,689.

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（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

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第六共同発明者の署名	日付	Sixth inventor's signature	Date
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国籍		Citizenship	
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住所		Residence	
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第十共同発明者の署名	日付	Tenth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	